GEORGE MASON UNIVERSITY

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

SPRING 2009

ECE 699: NanoCMOS and the Emergence of Nanoelectronics

Time and location: M 4:30-7:10 pm, ST2 Rm. 260
Instructor: Dimitris Ioannou, IN #247, tel. 993-1580, dioannou@gmu.edu
Office Hours: 3:00-4:00 pm; other times by appointment.

Textbook: J.P. Colinge, "Silicon on Insulator Technology", 3rd Ed., Springer (2004):
http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4020-7773-9

COURSE EMPHASIS

One third of this course will deal with the nanoCMOS MOSFET, including Silicon on Insulator (SOI) multi-gate MOSFETs and FinFETs. Moore's Law and the latest edition of the International Technology Roadmap for Semiconductors (ITRS, http://www.itrs.net) will be thoroughly discussed. In the second third of the course the fundamental, physics based limits to miniaturization and "ultimate" scaling will be discussed, which are applicable to all types of electronic devices, including the nanoCMOS MOSFET. The need thus will become apparent for "more than Moore" CMOS and the invention of new types of devices. The last third of the course will present a brief introduction of Nanoelectronics and discuss a couple of examples such as carbon nanotube (CNT) FETs and the single electron tunneling (SET) transistor. The course textbook given above contains much of the material that will be covered, but extensive use will be made of chapters from various other books as well as technical papers from the literature, which will be made available on the course webpage. The student in this class will be assumed to have a good understanding of modern physics as taught in typical undergraduate programs, and basic semiconductor device physics at a typical graduate (MS) level (i.e., as in the book by Muller and Kamins)

COURSE OUTLINE

1. Review of basic MOSFET theory
2. ITRS: http://www.itrs.net
3. SOI MOSFETs: Partially & Fully Depleted
4. SOI MOSFETs: Multi-Gate, FinFETs etc.
5. Natural length "λ" based scaling
6. Physics based limits to scaling
7. Introduction to Nanoelectronics
8. CNT FET, SET transistor, etc.

GRADING: midterm (30%), final (40%), project(s) (30%)